



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In Re Application of:

HOON KIM

Serial No.: 10/798,574

Examiner: DICKEY, THOMAS L

Filed: 12 March 2004

Art Unit: 2826

For: THIN FILM TRANSISTOR AND METHOD FOR FABRICATING THE SAME
WITH STEP FORMED AT CERTAIN LAYER (as amended)

INFORMATION DISCLOSURE STATEMENT

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

In accordance with 37 C.F.R. §1.56, and §§1.97 and 1.98 as amended, Applicant cites, describes, and provides copies of the following art references. Under 37 C.F.R. §1.98(a)(2) however, copies of U.S. patent reference(s) are not provided.

FOREIGN PATENT REFERENCE(S):

- Japanese Patent Publication No. 2001-320062 to Yoshinouchi, entitled *THIN FILM TRANSISTOR, ITS MANUFACTURING METHOD AND LIQUID CRYSTAL DISPLAY DEVICE*, published on 16 November 2001; and

Folio: P57012
Date: 12/11/06
I.D.: REB/ny

- Japanese Patent Publication No. 2002-033330 to Kasahara *et al.*, entitled *SEMICONDUCTOR DEVICE AND METHOD FOR MANUFACTURING THE SAME*, published on 31 January 2002,

OTHER DOCUMENT:

- *Office Action* from the Korean Intellectual Property Office issued in Applicant's corresponding Korean Patent Application No. 10-2003-0024431 dated 24 January 2005.

DISCUSSION

In the Korean Office action issued in Applicant's corresponding Korean patent application, the Examiner wrote that:

"The claims 1-7 in the present application are related to thin film transistor and a method thereof. A substrate, a buffer layer, an active layer, and a gate insulating layer are sequentially formed, and the buffer layer, wherein the gate insulating layer has a step between a lower part of the active layer and a part other than the lower part of the active layer, and the step is a half or less of the thickness sum of the active layer and the gate insulating layer."

and that:

" Claims 1-7 are obvious over the reference No. 1 (JP2001-320062) and the reference No. 2 (JP2002-33330) because the ordinary skilled person can make the claimed invention from the reference No. 1 (JP2001-320062) which discloses that a gate insulating film formed between a semiconductor layer and a gate electrode has a part for source/drain field and a part for a gate electrode, wherein the part for the gate electrode has 1.2 to 8 times as much thickness as the part for the source/drain field, and Fig. 6 of the reference No. 2 (JP2002-33330) which discloses the method of manufacturing a semiconductor device with the process of forming a stepped insulating layer which is formed on a substrate."

The citation of the foregoing references is not intended to constitute an assertion that other or more relevant art does not exist. Accordingly, the Examiner is requested to make a wide-ranging and thorough search of the relevant art.

Based upon the timeliness under 37 CFR §1.97(e)(1) of this filing of the Information Disclosure Statement and the Patent references from Japan cited in Korean Office action issued on the 24th January 2005, together with Applicant's Request for Continued Examination under 37 CFR §1.114(a)(1), no fee pursuant to 37 C.F.R. §1.97(d)(2) and 37 C.F.R. §1.17(e) is believed to be due; should this fee be due however, the Director is authorized to charge Deposit Account No. 02-4943 and to so notify Applicant's undersigned attorney.

Respectfully submitted,

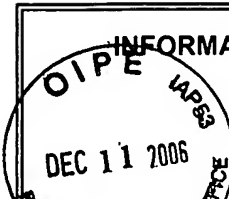
A handwritten signature in dark ink, appearing to read "R. E. Bushnell", is written over a horizontal line.

Robert E. Bushnell

Reg. No.: 27,774

1522 "K" Street, N.W., Suite 300
Washington, D.C. 20005
Area Code: (202) 408-9040

Folio: P57012
Date: 11 December 2006
I.D.: REB/ny

 INFORMATION DISCLOSURE STATEMENT PTO-1449 (PAGE 1 OF 1)	SERIAL NUMBER 10/798,574	DOCKET NO. P57012
	APPLICANT HOON KIM	
	FILING DATE 12 March 2004	GROUP 2826

U.S. PATENT DOCUMENTS

EXAMINER	DOCUMENT	DATE	NAME	CLASS	SUBCLASS	FILING DATE

FOREIGN PATENT DOCUMENTS

TRANSLATION

DOCUMENT	DATE	COUNTRY	CLASS	SUBCLASS	YES	NO
JP 2001-320062	11/16/01	JAPAN			Abstract	
JP 2002-033330	1/31/02	JAPAN			Abstract	

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, etc.)

	Office Action from the Korean Intellectual Property Office issued in Applicant's corresponding Korean Patent Application No. 10-2003-0024431 dated 24 January 2005.

EXAMINER:

DATE CONSIDERED:

EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP §609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.